VLSI Course Content:35hours

Course Outline

1. MOS Transistor Theory
1.1 Introduction
1.2 Ideal I-V Characterstics
1.3 C-V Characterstics
1.4 Nonideal I-V Effects
1.5 DC Transfer Characterstics
1.6 Switch -level RC Dealay Models

2. CMOS Processing Technology
2.1 Only Briefing

3. Circuit Performance Estimation
3.1 Delay Estimation
3.2 Logical Effort and Transistor Sizing
3.3 Power Dissipation
3.4 Interconnect
3.5 Design Margin

4. Combinational Circuit Design
4.1 Introduction
4.2 Circuit Famalies
4.3 Comparison of Circuit Families

5. Sequential Circuit Design
5.1 Sequencing Static Circuits
5.2 Circuit Designs of Latches and Flip Flops
5.3 Static Sequencing Element Theory
5.4 Syncnronizers

6. Datapath Subsystems
6.1 Addition and Substraction
6.2 One/Zero Detectors
6.3 Comparators
6.4 Synchronous Counter
6.5 Boolean Logical Operations
6.6 Codin
6.7 Parity
6.8 Multiplication
6.9 Division

7. Design Methodology and Tools
7.1 Platform Based Design
7.2 Design Flows
7.3 Design Economics

8. VHDL

8.1 Bahaviour Modelling with Concurrent Signal Assignments
8.2 Basic Constructs
8.3 Bahavioural Modeling with Process Statements
8.4 Finite State Machines
8.5 Parameterized Blocks